	STM32L1	**STM32L4**
ADC	ADC1	ADC1, ADC2, ADC3
	Max speed: 1 Msps	Max speed: 5.1 Msps (fast channel), 4.8 Msps (slow channel)
	12-bit	12-bit + digital oversampling up to 16-bit
	Reference Voltage: external	Reference Voltage: external (2.0 V to VDDA) or internal (2.048 V or 2.5 V)
	ADCCLK is always the HSI oscillator clock.	The ADCs clock can be derived (selected by software) from one of the three following sources: • system clock (SYSCLK), • PLLSAI1 VCO (PLLADC1CLK), • PLLSAI2 VCO (PLLADC2CLK).

	`typedef struct {`
	`__IO uint32_t SR;`
	`__IO uint32_t CR1;`
	`__IO uint32_t CR2;`
	`__IO uint32_t SMPR1;`
	`__IO uint32_t SMPR2;`
	`__IO uint32_t SMPR3;`
	`__IO uint32_t JOFR1;`
	`__IO uint32_t JOFR2;`
	`__IO uint32_t JOFR3;`
	`__IO uint32_t JOFR4;`
	`__IO uint32_t HTR;`
	`__IO uint32_t LTR;`
	`__IO uint32_t SQR1;`
	`__IO uint32_t SQR2;`
	`__IO uint32_t SQR3;`
	`__IO uint32_t SQR4;`
	`__IO uint32_t SQR5;`
	`__IO uint32_t JSQR;`
	`__IO uint32_t JDR1;`
	`__IO uint32_t JDR2;`
	`__IO uint32_t JDR3;`
	`__IO uint32_t JDR4;`
	`__IO uint32_t DR;`
	`} ADC_TypeDef;`
		`typedef struct{`
		`__IO uint32_t ISR;`
		`__IO uint32_t IER;`
		`__IO uint32_t CR;`
		`__IO uint32_t CFGR;`
		`__IO uint32_t CFGR2;`
		`__IO uint32_t SMPR1;`
		`__IO uint32_t SMPR2;`
		`__IO uint32_t TR1;`
		`__IO uint32_t TR2;`
		`__IO uint32_t TR3;`
		`__IO uint32_t SQR1;`
		`__IO uint32_t SQR2;`
		`__IO uint32_t SQR3;`
		`__IO uint32_t SQR4;`
		`__IO uint32_t DR;`
		`__IO uint32_t JSQR;`
		`__IO uint32_t OFR1;`
		`__IO uint32_t OFR2;`
		`__IO uint32_t OFR3;`
		`__IO uint32_t OFR4;`
		`__IO uint32_t JDR1;`
		`__IO uint32_t JDR2;`
		`__IO uint32_t JDR3;`
		`__IO uint32_t JDR4;`
		`__IO uint32_t AWD2CR;`
		`__IO uint32_t AWD3CR;`
		`__IO uint32_t DIFSEL;`
		`__IO uint32_t CALFACT;`
		`} ADC_TypeDef;`
		
		typedef struct {
		__IO uint32_t CSR;
		__IO uint32_t CCR;
		__IO uint32_t CDR;
		} **ADC_Common**_TypeDef;